INTEGRATED CIRCUITS

DATA SHEET

TDA8421

Hi-fi stereo audio processor; I^2C bus

Product specification
File under Integrated Circuits, IC02

May 1988

Philips Semiconductors

PHILIPS

Hi-fi stereo audio processor; I^2C bus TDA8421

GENERAL DESCRIPTION

The TDA8421 is a monolithic bipolar integrated stereo sound circuit with a loudspeaker channel (CH1) and a headphone channel (CH2), digital controlled via the I^2C bus, for application in hi-fi audio and television sound.

Features

- Input selector
- Mode selector
- Loudspeaker channel (CH1); with volume control, balance control and mute
- Headphone channel (CH2); with volume control, balance control and mute
- Pseudo stereo and spatial function
- Bass and treble control
- Electrostatic discharge protection diodes

QUICK REFERENCE DATA

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Input signal handling	V_I	2	–	–	V
Input sensitivity					
full power at the output stage	V_i	–	200	–	mV
Signal plus noise-to-noise ratio	(S+N)/N	–	90	–	dB
Total harmonic distortion	THD	–	0,05	–	%
Channel separation	α	–	75	–	dB
Volume control range CH1	G	–62	–	16	dB
Treble control range	G	–12	–	12	dB
Bass control range	G	–12	–	15	dB
Volume control range CH2	G	–62	–	0	dB

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT117); SOT 117-1; 1996 november 19.

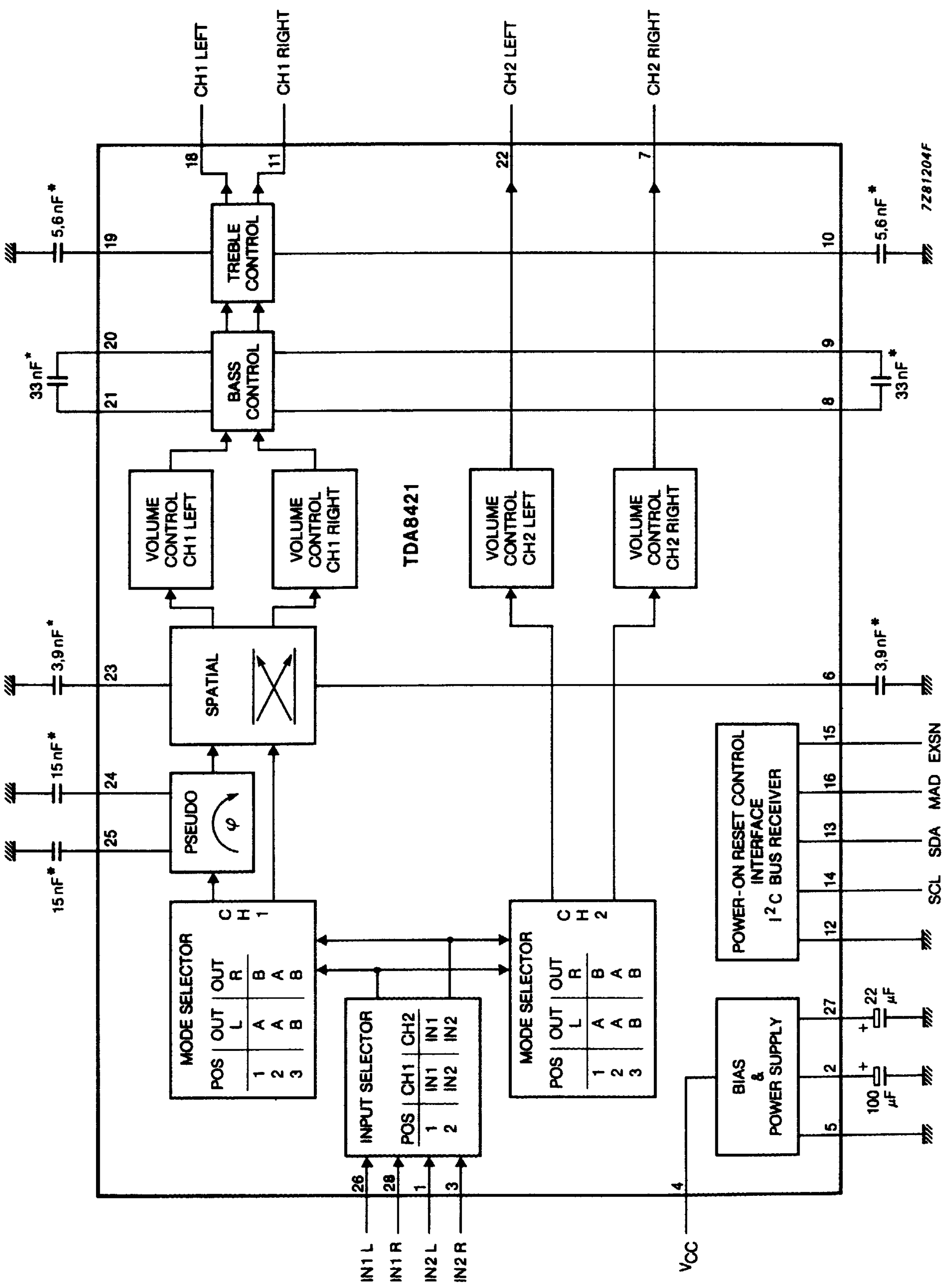


Fig.1 Block diagram.

* These values are dependent on the required frequency response and effect.

PINNING

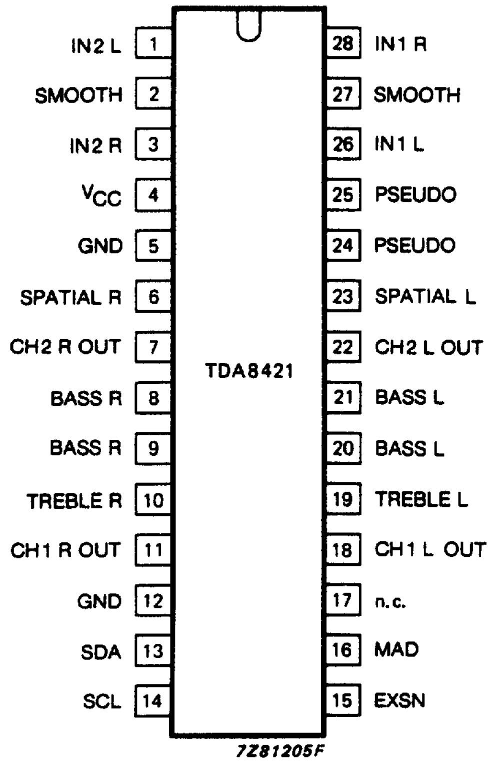


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Input selector

The input to channel 1 (CH1) and channel 2 (CH2) is determined by the input selector. The selection is made from the following AF input signals:

- IN1 L (pin 26); IN1 R (pin 28) or
- IN2 L (pin 1); IN2 R (pin 3)

Where IN1 is an internal input signal and IN2 an external input signal.

Mode selector

For each channel (CH1 and CH2) there is a mode selector which selects between stereo, sound A and sound B in the event of bilingual transmission. Both mode selectors can be controlled independently.

Headphone channel (CH2)

Volume control and balance

The stages for volume control for CH2 consist of two parts for left and right. In each part the gain can be adjusted between 0 and –62 dB in steps of 2 dB. An additional step allows an attenuation of ≥ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Loudspeaker channel (CH1)

Volume control and balance

The loudspeaker channel (CH1) also consists of two parts for volume control (left and right). In each part the gain can be adjusted between + 16 dB and –62 dB in steps of 2 dB. An additional step allows an attenuation of ≥ 90 dB. Both parts can be controlled independently over the whole range, which allows the balance to be varied by controlling the volume of left and right.

Stereo/pseudo stereo/spatial stereo mode

It is possible to select three modes. Stereo, pseudo or spatial stereo. The pseudo stereo mode receives mono transmissions and the stereo and spatial stereo mode receives stereo transmissions.

Bass control

The bass control stage can be switched from an emphasis of 15 dB to an attenuation of 12 dB for low frequencies in steps of 3 dB.

Treble control

The treble control stage can be switched from + 12 dB to –12 dB in steps of 3 dB.

Bias and power supply

The TDA8421 includes a bias and power supply stage, which generates a voltage of ½ V_{CC} with a low output impedance and injector currents for the logic part.

Power-on reset

The on-chip power-on reset circuit sets the mute bit to active, which mutes both the loudspeaker channel (CH1) and the headphone channel (CH2). The muting can be switched by transmission of the mute bit.

I^{2}C bus receiver and data handling

Bus specification

The TDA8421 is controlled via the 2-wire I^{2}C bus by a microcomputer. The two wires (SDA - serial data, SCL - serial clock) carry information between the devices connected to the bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor.
When the bus is free both lines are HIGH. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The set up and hold times are specified in AC CHARACTERISTICS.

A HIGH-to-LOW transition of the SDA line while SCL is HIGH is defined as a start condition. A LOW-to-HIGH transition of the SDA line while SCL is HIGH is defined as a stop condition. The bus receiver will be reset by the reception of a start condition. The bus is considered to be busy after the start condition. The bus is considered to be free again after a stop condition.

Module address

Data transmission to the TDA8421 starts with the module address MAD.

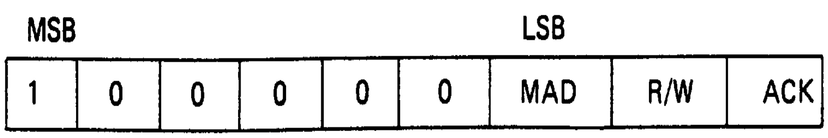


Fig.3 TDA8421 module address.

The module address is determined by pin 16. When connected to ground MAD = 0; when connected to V_{CC} MAD = 1. Thus two TDA8421s can be selected within a system.

Subaddress

After the module address byte a second byte is used to select the functions for both channels:

- CH1 - Volume left, volume right, bass, treble and switch functions
- CH2 - Volume left, volume right and switch functions

The subaddress SAD is stored within the TDA8421. Table 1 defines the coding of the second byte after the module address MAD.

Table 1 Second byte after module address MAD

		128	64	32	16	8	4	2	1
		MSB							**LSB**
	FUNCTION	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CH1	volume left	0	0	0	0	0	0	0	0
	volume right	0	0	0	0	0	0	0	1
	bass	0	0	0	0	0	0	1	0
	treble	0	0	0	0	0	0	1	1
	switch functions	0	0	0	0	1	0	0	0
CH2	volume left	0	0	0	0	0	1	0	0
	volume right	0	0	0	0	0	1	0	1
	switch functions	0	0	0	0	1	1	0	0
						subaddress SAD			

Definition of 3rd byte

A third byte is used to transmit data to the TDA8421. Table 2 defines the coding of the third byte after module address MAD and subaddress SAD.

Table 2 Third byte after module address MAD and subaddress SAD

			MSB							**LSB**
	FUNCTION		**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CH1	volume left	VL1	1	1	V05	V04	V03	V02	V01	V00
	volume right	VR1	1	1	V15	V14	V13	V12	V11	V10
	bass	BA	1	1	1	1	BA3	BA2	BA1	BA0
	treble	TR	1	1	1	1	TR3	TR2	TR1	TR0
	switch functions	S1	1	1	MU	EFL	STL	ML1	ML0	IS
CH2	volume left	VL2	1	1	V25	V24	V23	V22	V21	V20
	volume right	VR2	1	1	V35	V34	V33	V32	V31	V30
	switch functions	S2	1	1	1	1	EXS	MH1	MH0	1

Truth tables

Truth tables for the switch functions

Table 3 Input selector

function	IS
IN1	0
IN2	1

Table 4 Mode selectors

mode	CH1		CH2	
	ML0	ML1	MH0	MH1
stereo	1	1	1	1
sound A	1	0	1	0
sound B	0	1	0	1
----------	0	0	0	0

Table 5 Stereo/pseudo stereo/spatial stereo

choise	STL	EFL
spatial	1	1
stereo	1	0
pseudo	0	1
-----------	0	0

Table 6 Mute

mute	MU
active; automatic after POR(1)	1
not active	0

Notes

1. Attenuation ≥ 90 dB; POR = Power-On Reset.

Table 7 Output for external switch

EXSN	EXS
ground	1
open collector	0

Truth tables for the volume base and treble controls.

Table 8 Volume control

CH1	CH2	V × 5	V × 4	V × 3	V × 2	V × 1	V × 0
16	0	1	1	1	1	1	1
14	–2	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
–46	–62	1	0	0	0	0	0
–48	≤–90	0	1	1	1	1	1
.	.	.	.	.	.	.	.
–62	≤–90	0	1	1	0	0	0
≤–90	≤–90	0	1	0	1	1	1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
≤–90	≤–90	0	0	0	0	0	0

Note

1. The values of CH1 and CH2 are in 2 dB/step measured in dBs.

Table 9 Bass control

3dB/STEP (dB)	BA3	BA2	BA1	BA0
15	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
15	1	0	1	1
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
–12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
–12	0	0	0	0

Table 10 Treble control

3dB/STEP (dB)	TR3	TR2	TR1	TR0
12	1	1	1	1
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
12	1	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
0	0	1	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
–12	0	0	1	0
---	---	---	---	---
---	---	---	---	---
---	---	---	---	---
–12	0	0	0	0

Sequence of data transmission

After a power-on reset all eight functions have to be adjusted with eight data transmissions. It is recommended that data information for switch functions in CH1 are transmitted last because all functions have to be adjusted when the muting is switched off. The sequence of transmission of other data information is not critical.

The order of data transmission is shown in Figures 4 and 5. The number of data transmissions is unrestricted but before each data byte the module address MAD and the correct subaddress SAD is required.

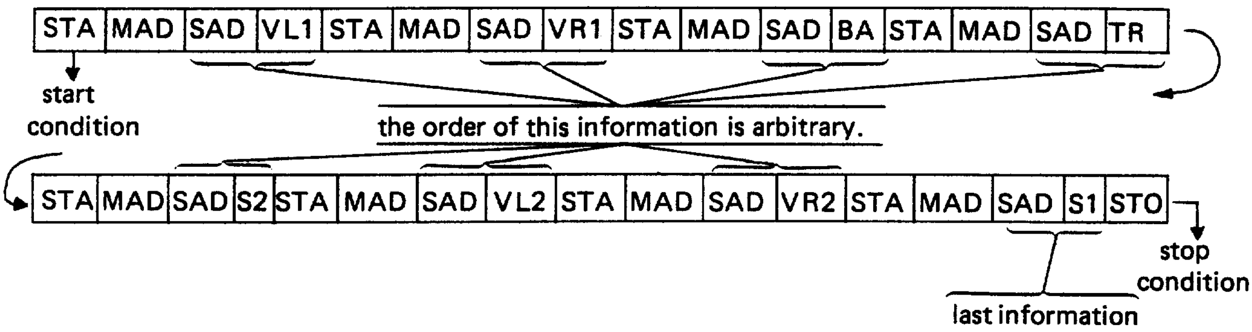


Fig.4 Data transmission after a power-on reset.

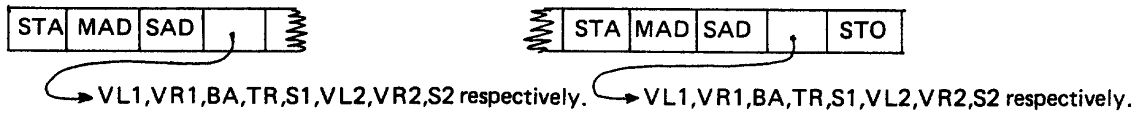


Fig.5 Data transmission except after power-on reset.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply voltage	V_{CC}	0	16	V
Voltage range at pins for external capacitors				
pins 2, 6, 8 to 10, 19 to 21, 23 to 25, 27	V_{cap}	0	V_{CC}	V
pin 13	V_{SDA}	0	V_{CC}	V
pin 14	V_{SCL}	0	V_{CC}	V
pin 15	V_{EXSN}	0	V_{CC}	V
pin 16	V_{MAD}	0	V_{CC}	V
Voltage range				
at pins 1, 3, 7, 11, 18, 22, 26, 28	V_I, V_O	0	V_{CC}	V
Output current at pins 7, 11, 18, 22	I_O	–	45	mA
Total power dissipation				
at T_{amb} < 70 °C	P_{tot}	–	1350	mW
Operating ambient temperature range	T_{amb}	0	70	°C
Storage temperature range	T_{stg}	–25	150	°C
Electrostatic handling(1)	$\pm V_{ESD}$	–	2000	V

Note

1. Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ resistor.

DC CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (pin 4)	V_{CC}	7,5	12	14	V
Supply current					
at V_{CC} = 12 V	I_{CC}	–	42	55	mA
Internal input voltage					
IN1 L,R (pins 26,28) IN2 L,R (pins 1,3) DC voltage internally generated; capacitive coupling recommended	V_I	5,4	6,0	6,6	V
MAD (pin 16)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	0	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	µA
input current LOW	I_{IL}	–	1	10	µA
SDA; SCL (pins 13 and 14)					
input voltage HIGH	V_{IH}	3,0	–	V_{CC}	V
input voltage LOW	V_{IL}	–0,3	–	1,5	V
input current HIGH	I_{IH}	–	–	1,0	µA
input current LOW	I_{IL}	–	1	10	µA
Output voltage at					
CH1 (pins 11 and 18); CH2 (pins 7 and 22)	V_O	5,4	½ V_{CC}	6,6	V
pins with external capacitors					
pins 6 to 10; 19 to 21; 23 to 25	$V_{cap.n}$	–	½ V_{CC}	–	V
pin 2	$V_{cap.2}$	–	V_{CC}–0,1	–	V
External switch (pin 15)					
at I_{EXSN} = 1 mA					
Output voltage HIGH	V_{EXSNH}	–	–	16	V
Output voltage LOW	V_{EXSNL}	–	–	0,3	V

AC CHARACTERISTICS

V_{CC} = 12 V; bass/treble in linear position; pseudo and spatial stereo off; R_L > 10 kΩ; C_L < 100 pF; T_{amb} = 25 °C unless otherwise specified.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
I²C bus timing (see Fig.6)					
SDA, SCL (pin 13 and 14)					
Clock frequency range	f_{SCL}	0	–	100	kHz
The HIGH period of the clock	t_{HIGH}	4	–	–	µs
The LOW period of the clock	t_{LOW}	4,7	–	–	µs
SCL rise time	t_r	–	–	1	µs
SCL fall time	t_f	–	–	0,3	µs
Set-up time for start condition	$t_{SU;STA}$	4,7	–	–	µs
Hold time for start condition	$t_{HD; STA}$	4	–	–	µs
Set-up time for stop condition	$t_{SU; STO}$	4,7	–	–	µs
Time bus must be free before a new transmission can start	t_{BUF}	4,7	–	–	µs
Set-up time DATA	$t_{SU; DAT}$	250	–	–	ns
Input signals					
IN1 L (pin 26) IN1 R (pin 28)					
IN2 L (pin 1) IN2 R (pin 3)					
Input signal handling (r.m.s. value) at V_u = –4 dB; THD ≤ 0,5%	$V_{i(rms)}$	2	–	–	V
Input resistance	R_{n-5}	35	50	–	kΩ
Frequency response (–0,5 dB) bass and treble in linear position; stereo mode; effects off	f	20	–	20 000	Hz

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
LOUDSPEAKER CHANNEL OUTPUTS					
CH1 LEFT (pin 18); CH1 RIGHT (pin 11)					
Output voltage range (r.m.s. value)					
at THD ≤ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level					
weighted according to CCIR468-2					
gain = 16 dB	V_n	–	90	–	μV
gain = 0 dB	V_n	–	20	40	μV
gain = ≤ –90 dB	V_n	–	15	–	μV
Total harmonic distortion					
(f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,5 V; gain = + 16 dB to –30 dB	THD	–	0,05	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = +2 dB to –30 dB	THD	–	0,07	0,2	%
for $V_{i(rms)}$ = 2,0 V; gain = –4 dB to –30 dB	THD	–	0,1	–	%
Channel separation at 10 kHz					
gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB;					
bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic					
inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
VOLUME CONTROL					
For truth table see Table 8					

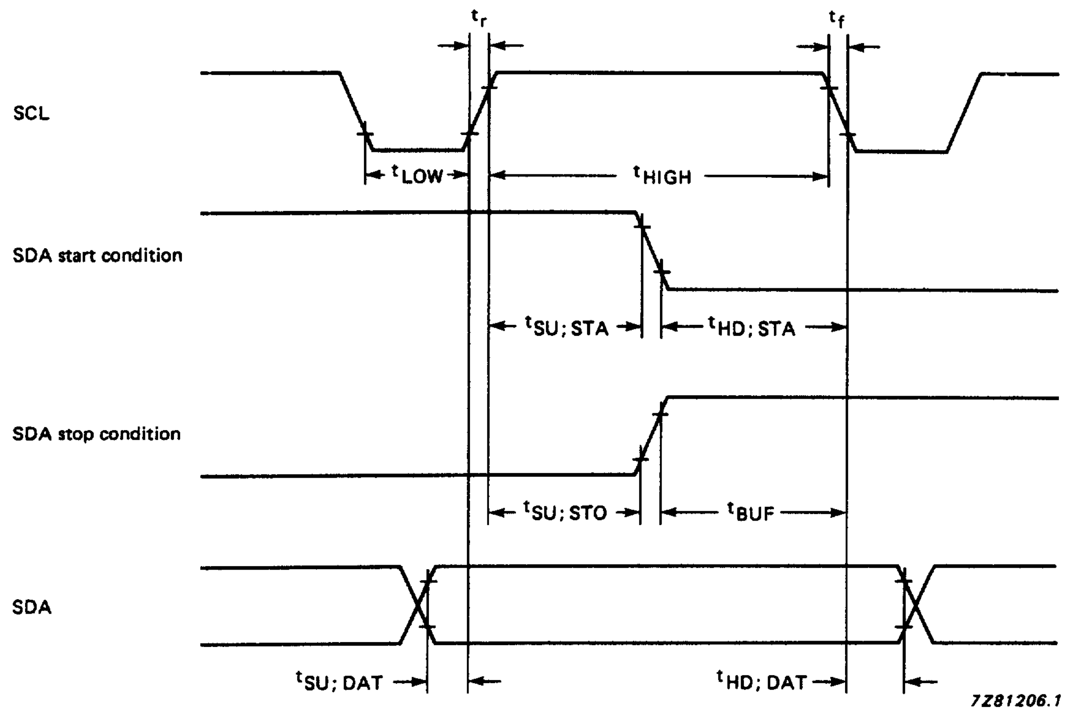
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Loudspeaker channel (CH1)					
Control range at f = 1 kHz					
maximum voltage gain (16 dB step)	G_{max}	15	–	–	dB
minimum voltage gain (–62 dB step)	G_{min}	–60	–	–	dB
last position	G_{off}	–80	–85	–	dB
mute position	G_{mute}	–85	–90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 16 dB to –30 dB	ΔG	–	–	0,5	dB
gain from –30 dB to –62 dB	ΔG	–	–	1	dB
TREBLE CONTROL (CH1)					
For truth table see Table 10					
Control range					
for $C_{10\text{-}5}$; $C_{19\text{-}5}$ = 5,6 nF					
Maximum emphasis at 15 kHz with respect to linear position	G	11	12	13	dB
Maximum attenuation at 15 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
BASS CONTROL					
For truth table see Table 9					
Control range					
for $C_{8\text{-}9}$; $C_{20\text{-}21}$ = 33 nF					
Maximum emphasis at 40 kHz with respect to linear position	G	14	15	16	dB
Maximum attenuation at 40 kHz with respect to linear position	G	11	12	13	dB
Resolution	G_{step}	–	3	–	dB/step
SPATIAL AND PSEUDO FUNCTION					
Spatial:					
Antiphase crosstalk	α	–	50	–	%
Pseudo:					
Phase shift (see Fig.15)					

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
HEADPHONE CHANNEL OUTPUTS					
CH2 LEFT (pin 22); CH2 RIGHT (pin 7)					
Output voltage range (r.m.s. value)					
at THD ≤ 0,5%	$V_{o(rms)}$	2	–	–	V
Load resistance	R_L	10	–	–	kΩ
Output impedance	Z_O	–	–	100	Ω
Noise level					
(weighted according to CCIR468-2) gain = 0 dB	V_n	–	15	–	μV
gain = 16 dB	V_n	–	12	25	μV
gain = ≤ –90 dB	V_n	–	10	–	μV
Total harmonic distortion					
(f = 20 Hz to 12,5 kHz)					
for $V_{i(rms)}$ = 0,2 V; gain = 0 dB to –30 dB	THD	–	0,01	0,2	%
for $V_{i(rms)}$ = 1,0 V; gain = 0 dB to –30 dB	THD	–	0,1	–	%
for $V_{i(rms)}$ = 2,0 V gain = –4 dB to –30 dB	THD	–	0,3	–	%
Channel separation at 10 kHz					
gain = 0 dB	α_{cr}	–	75	–	dB
Ripple rejection (gain = 0 dB;					
bass and treble in linear position) f_{ripple} = 100 Hz	RR_{100}	–	50	–	dB
Crosstalk attenuation from logic					
inputs to AF outputs (gain = 0 dB; bass and treble in linear position)	α_L	–	110	–	dB
Crosstalk between any input/output					
f = 100 Hz to 12,5 kHz	α	65	70	–	dB
Crosstalk IN1/IN2					
gain = 0 dB; R_G = 0	α	95	100	–	dB

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Headphone channel (CH2)					
Control range					
maximum voltage gain (0 dB step)	G_{max}	–1	–	–	dB
minimum voltage gain (–62 dB step)	G_{min}	–57	–	–	dB
last position	G_{off}	–80	–85	–	dB
mute position	G_{mute}	–85	–90	–	dB
Resolution	G_{step}	–	2	–	dB/step
Gain difference between left and right AF channel (note 1)					
gain from 0 dB to –40 dB	ΔG	–	–	0,5	dB
gain from –40 dB to –62 dB	ΔG	–	–	2	dB

Note to the AC characteristics

1. Balance is realized via software by different volume settings in both channels.



$t_{SU;\,STA}$ = start code set-up time
$t_{HD;\,STA}$ = start code hold time
$t_{SU;\,STO}$ = stop code set-up time

t_{BUF} = BUS free time
$t_{SU;\,DAT}$ = data set-up time
$t_{HD;\,DAT}$ = DATA hold time

Fig.6 Timing requirements for I ^{2} C bus.

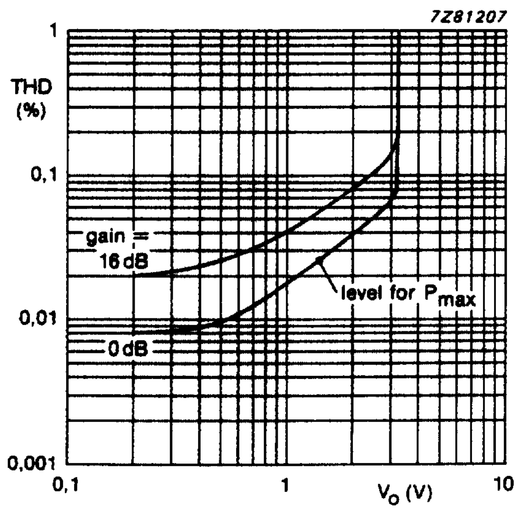


Fig.7 Distortion loudspeaker channel CH1 as a function of the output voltage with gain as parameter.

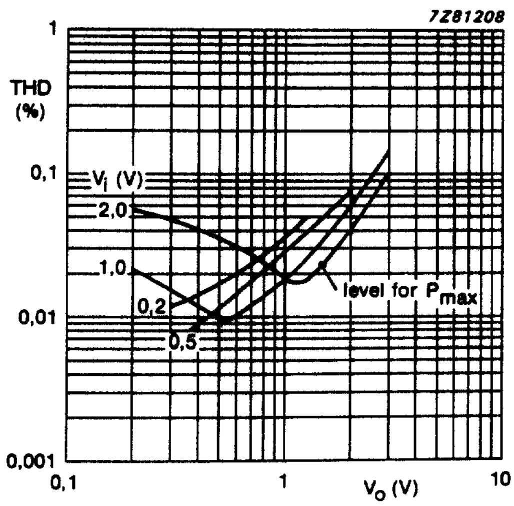


Fig.8 Distortion loudspeaker channel CH1 as a function of the output voltage with input voltage as parameter.

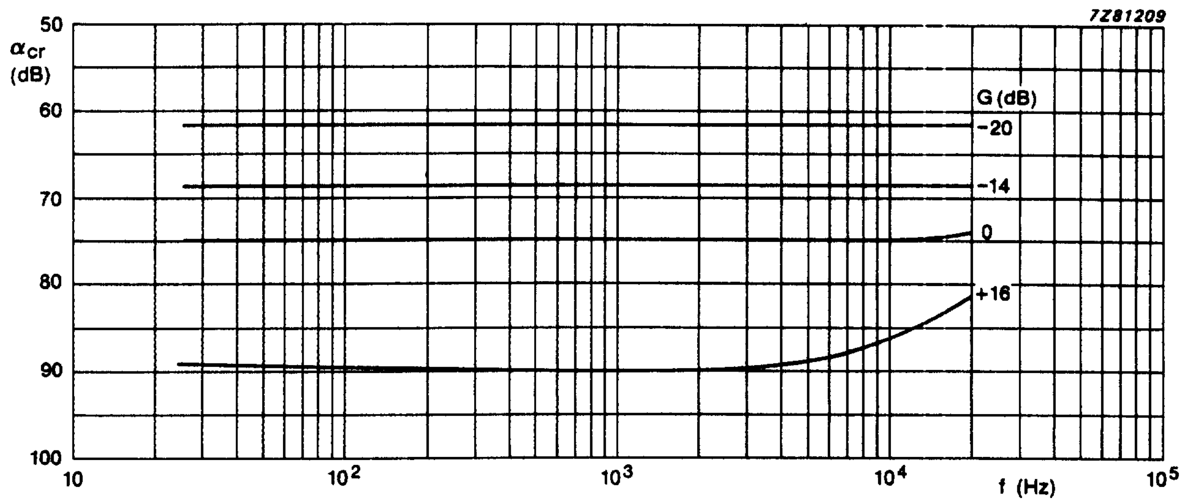


Fig.9 Channel separation loudspeaker channel CH1 as a function of frequency.

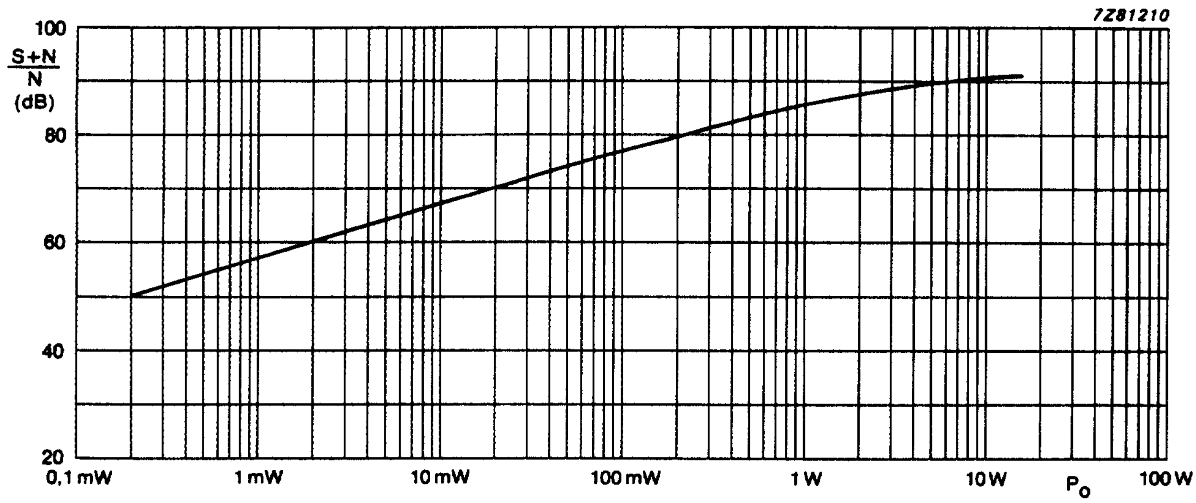


Fig.10 Signal-to-noise ratio as a function of output power.
Input voltage V_i = 0,5 V; according to CCIR; quasi peak; P_o = 15 W.

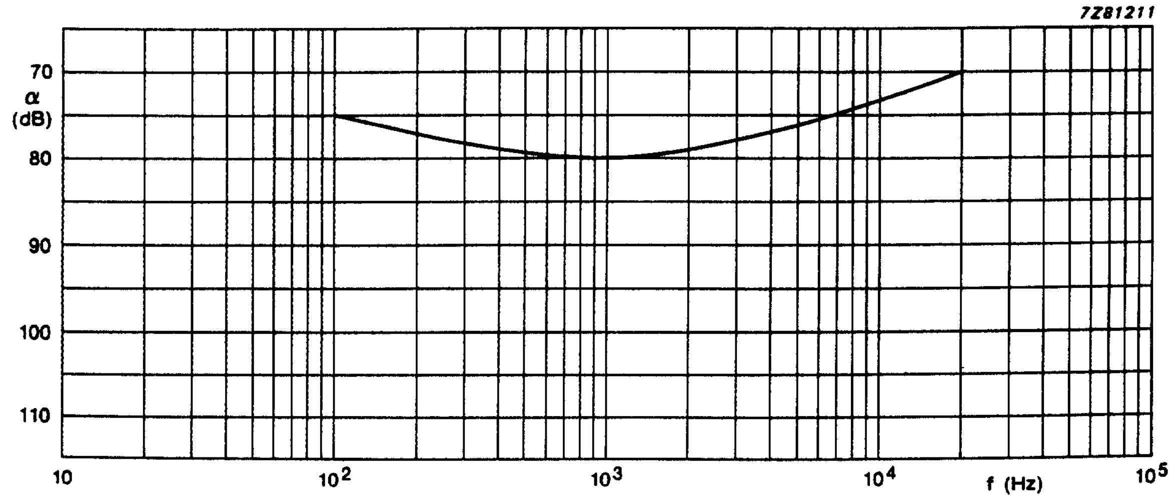


Fig.11 Crosstalk 2-tone mode as a function of frequency.
CH1: mode AA, Gain + 16 dB; CH2: mode BB, Gain 0 dB.
Signal input RIGHT; input LEFT to ground, measured at output CH1.

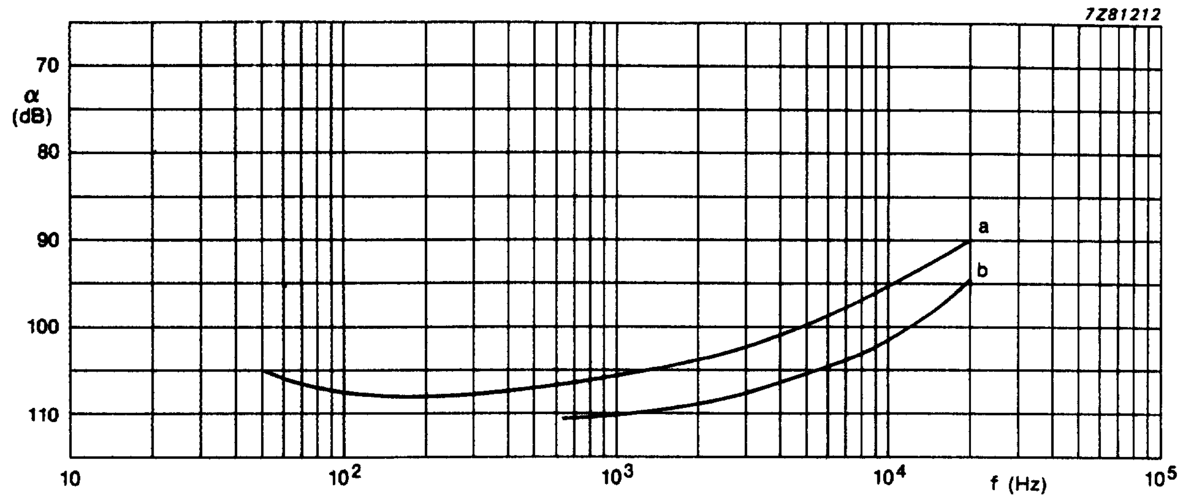


Fig.12 Crosstalk between IN1 and IN2 as a function of frequency; measured at output CH1; R_G = 0.
a) Gain = + 16 dB; V_i = 200 mV. b) Gain = 0 dB; V_i = 1 V.

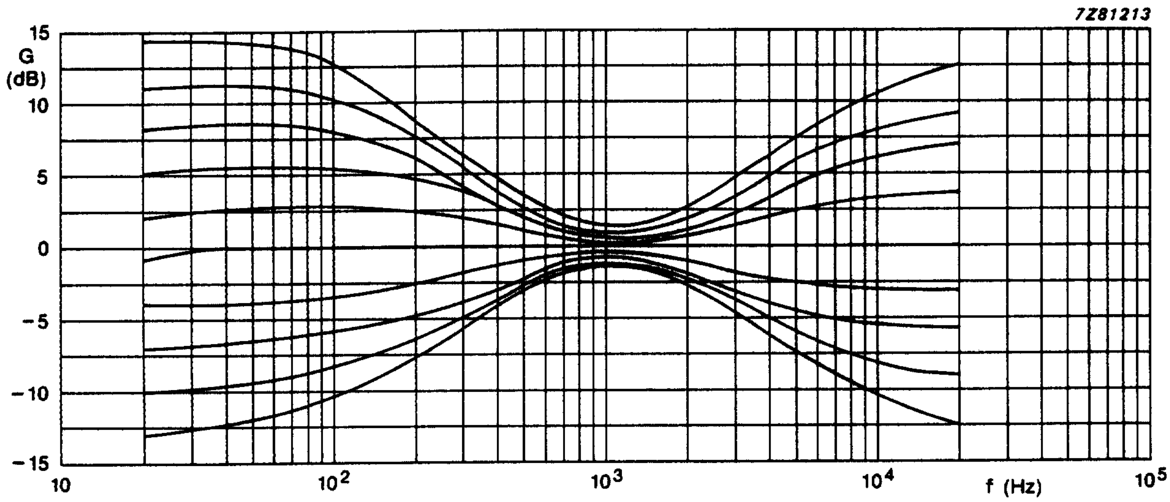


Fig.13 Bass and treble tone control. C_{bass} = 33 nF, C_{treble} = 5,6 nF.

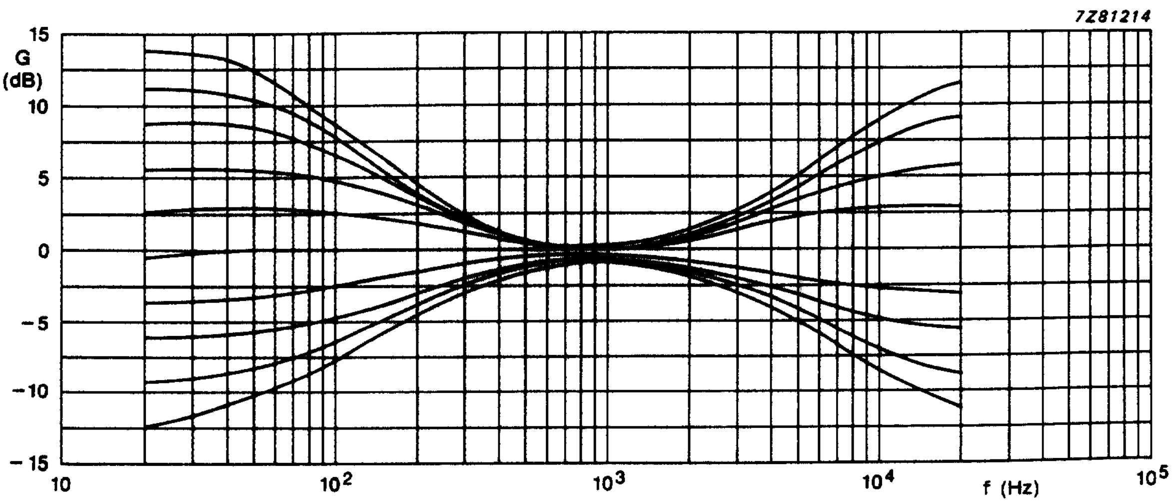


Fig.14 Bass and treble tone control. C_{bass} = 68 nF, C_{treble} = 3.9 nF.

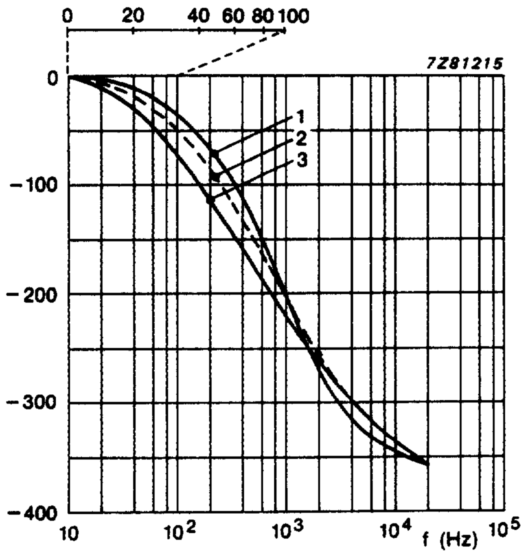


Fig.15 Pseudo (phase) as a function of frequency CH 1 left.

CURVE	PIN 24 (nF)	PIN (nF)	EFFECT
1	15	15	normal
2	5,6	47	intensified
3	5,6	68	more intensified

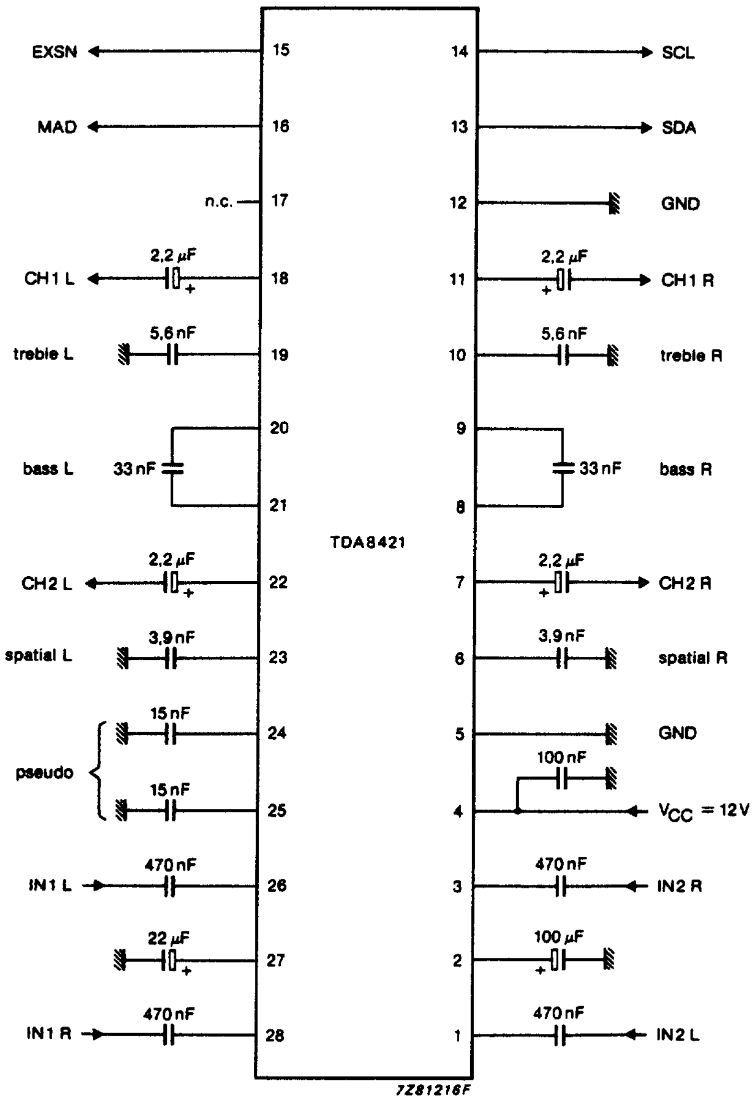
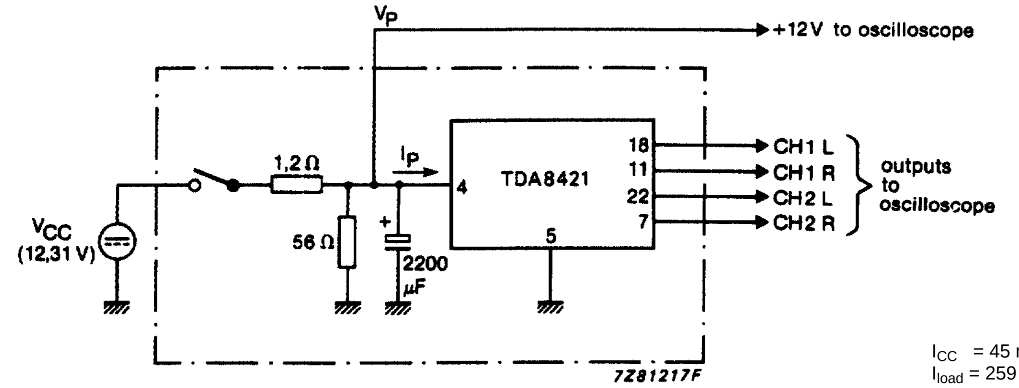


Fig.16 Test and application circuit diagram.



I_{CC} = 45 mA;
I_{load} = 259 mA;
t_{on} = 2,64 ms;
t_{off} = 102 ms.

Fig.17 Turn-on/off power supply circuit diagram.

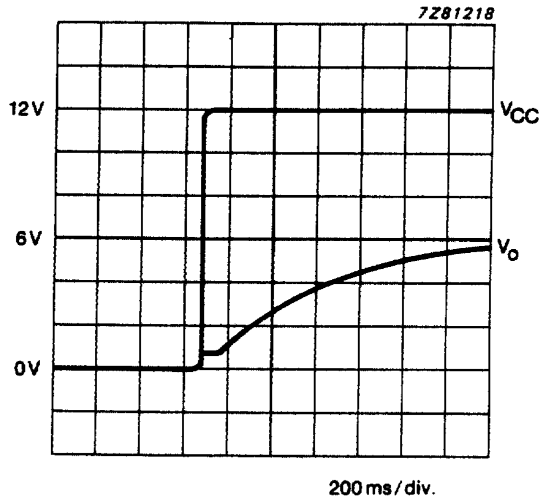


Fig.18 Turn-on behaviour;
C = 2,2 μF; R_L = 10 kΩ.

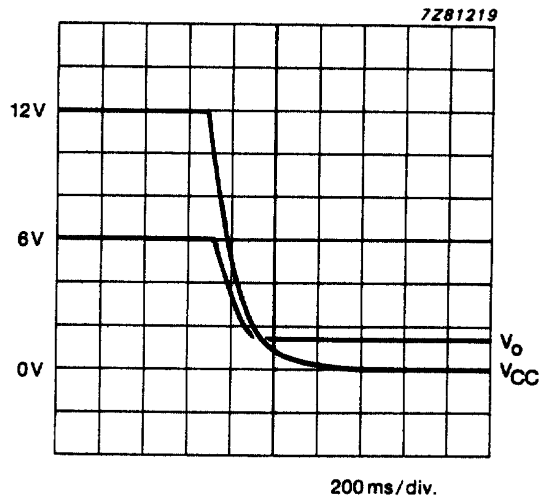


Fig.19 Turn-off behaviour; without modulation.

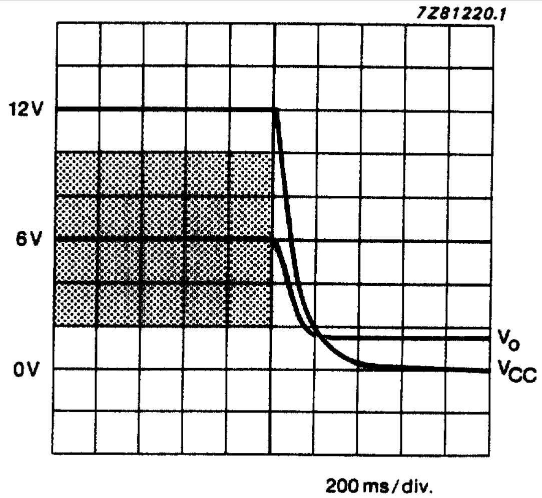


Fig.20 Turn-off behaviour; with modulation (shaded area).

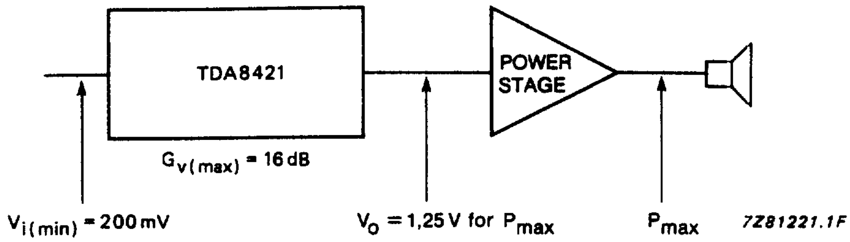


Fig.21 Level diagram loudspeaker channel CH1 with $V_{i(min)}$ = 200 mV; V_o = 1,25 for P_{max}.

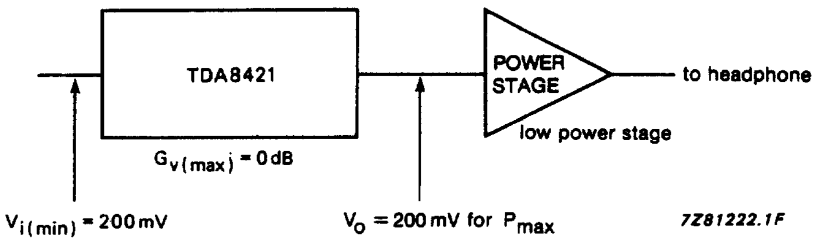
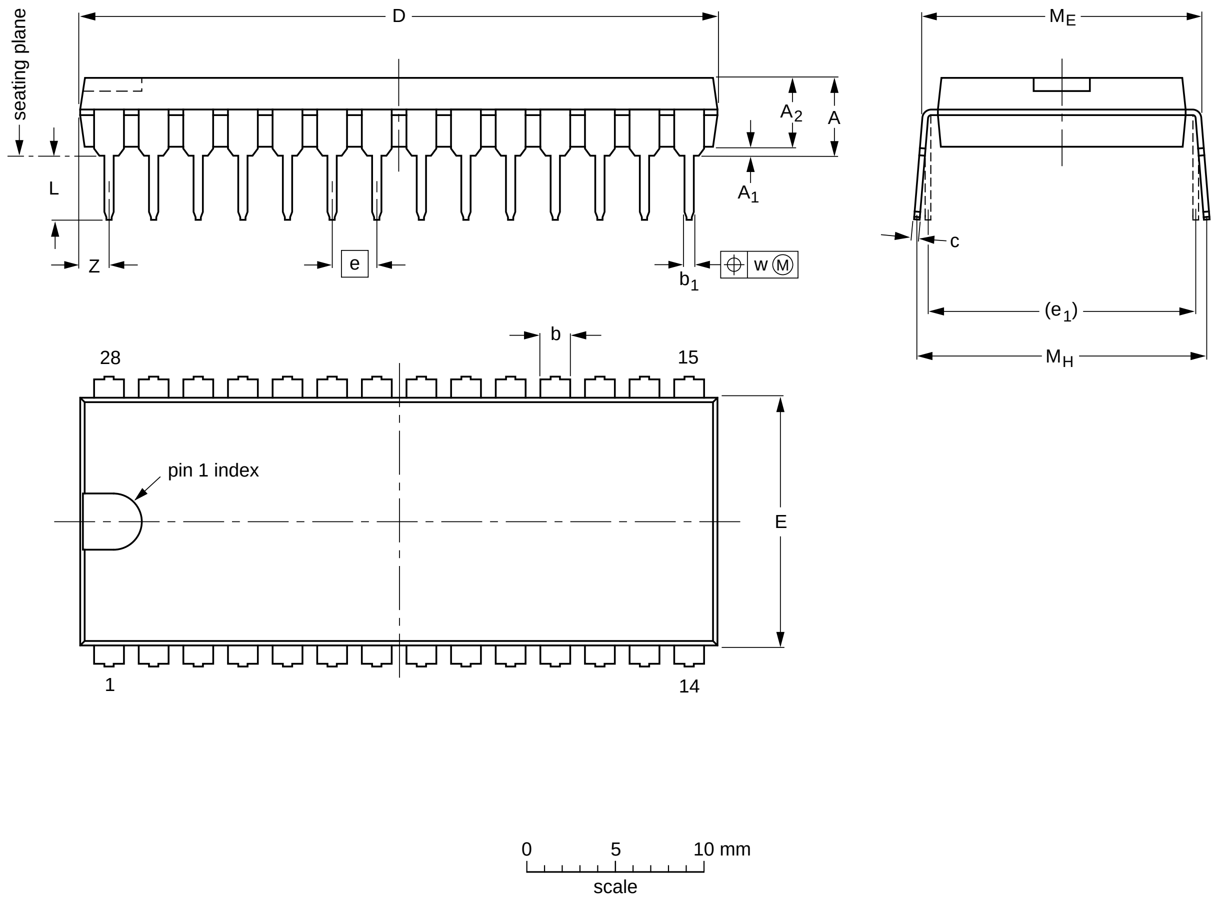


Fig.22 Level diagram headphone channel CH2 with V_i = 200 mV; V_o = 200 mV for P_{max}.

PACKAGE OUTLINE

DIP28: plastic dual in-line package; 28 leads (600 mil) — SOT117-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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